In re Patent Application of:
ROCHE ET AL.
Serial No. **09/995,251**
Filing Date: **NOVEMBER 27, 2001**

REMARKS

The Examiner is thanked for the thorough examination of the present application, for allowing Claims 45-53, and for identifying allowable subject matter in Claims 20, 21, 23, 30, 31, 33, 40, 42, 57, 58, and 60. The Examiner is also thanked for properly withdrawing the prior rejection and not making the present rejection final. Claims 19, 23, 29, 33, 39, 45, 48, and 60 were amended to correct minor typographical errors. Independent Claim 54 has been amended to further define the invention over the prior art. New dependent Claim 63 has been added.

The patentability of the claims is discussed in greater detail below. Favorable reconsideration is respectfully requested.

I. The Claimed Invention

Independent Claim 15, for example, is directed to a microprocessor comprising a first terminal for receiving a mode selection signal, and a second terminal for receiving a control signal. The microprocessor further comprises selection means connected to the first and second terminals for selecting an operating mode of the microprocessor based upon the mode selection signal and the control signal. The selection means comprises a counter having a counting input and a reset input, with first coupling means coupling the counting input to the first terminal. The selection means also comprises second coupling means coupling the reset input to the second terminal, and default means for maintaining by default the reset input at a first logic value for ensuring that the counter is maintained at zero in an absence of the

control signal.

Independent Claim 26 is similar to Claim 15, but recites the structure of the circuit. Independent Claim 36 is a method counterpart of Claim 26 and includes similar recitations.

Amended independent Claim 54 is directed to a microprocessor comprising a line receiving a reset signal having an active state during a resetting period of the microprocessor, and a first terminal for receiving a mode selection signal. The microprocessor also comprises a second terminal for receiving a control signal that is different from the reset signal, and a selection circuit connected to the first and second terminals for selecting a mode of the microprocessor based upon the mode selection signal and the control signal. The selection circuit comprises a counter having a counting input and a reset input, a first coupling circuit coupling the counting input to the first terminal, and a second coupling circuit coupling the reset input to the second terminal. The second coupling circuit comprises an output coupled to the reset input of the counter, a first input coupled to the second terminal, and a second input for receiving an inhibit signal for inhibiting the output of the second coupling circuit when the first input receives the control signal outside a selection period for selecting a mode of the microprocessor. The selection period corresponds to a period when the reset signal is in the active state. The second coupling circuit also comprises a device for maintaining the reset input at a first logic value for ensuring that the counter is maintained at a predetermined value in an absence of the control signal.

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II. Claims 15-44 Are Patentable

The Examiner rejected independent Claims 15, 26, and 36 as unpatentable over the admitted prior art in view of the Farnworth et al. patent. The Examiner notes the admitted prior art fails to disclose default means for maintaining by default the reset input at a first logic value for ensuring that the counter is maintained at zero in an absence of the control signal. The Examiner notes the Farnworth et al. patent discloses default means comprising the switching circuit, impedance circuit, and voltage circuit of FIG. 6A for ensuring an IC device does not accidentally enter a test mode of operation by holding a test mode determining signal at a constant value.

In contrast, independent Claim 15, for example, recites default means for maintaining by default the reset input at a first logic value for ensuring that the counter is maintained at zero in an absence of the control signal. In other words, not only does the default means maintain the reset input at a first logic value, the default means also ensures that the counter is maintained at zero in the absence of the control signal. The Farnworth et al. patent fails to supply this noted deficiency because the Examiner's selected test mode determining signal fails to ensure that a counter is maintained at zero in the absence of the control signal. Independent Claims 26 and 36 include similar recitations to Claim 15.

Accordingly, independent Claims 15, 26, and 36 are patentable. The dependent claims, which recite yet further

distinguishing features of the invention, are also patentable, and require no further discussion.

III. Claims 54-63 Are Patentable

The Examiner rejected independent Claim 54 as unpatentable over the admitted prior art in view of the Farnworth et al. patent. The admitted prior art and the Farnworth et al. patent are discussed above.

Amended independent Claim 54 is directed to a microprocessor comprising a line receiving a reset signal having an active state during a resetting period of the microprocessor, a second terminal for receiving a control signal that is different from the reset signal, and a second coupling circuit coupling the reset input to a second terminal. The second coupling circuit comprises a first input and a second input for receiving an inhibit signal for inhibiting the output of the second coupling circuit when the first input receives the control signal outside a selection period for selecting a mode of the microprocessor. The selection period corresponds to a period when the reset signal is in the active state. In other words, the microprocessor has a reset signal having an active state that defines the beginning and the end of a mode selection period, and the control signal is different than the reset signal. Even the selective combination of the admitted prior art and the Farnworth et al. patent fails to disclose such.

Accordingly, independent Claim 54 is patentable. Its dependent claims, which recite yet further distinguishing features of the invention, are also patentable, and require no further discussion.

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IV. CONCLUSION

In view of the amendments to Claim 54 and the arguments provided herein, it is submitted that all the claims are patentable. Accordingly, a Notice of Allowance is requested in due course. Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned at the telephone number listed below.

Respectfully submitted,

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CERTIFICATE OF FACSIMILE TRANSMISSION

I HEREBY CERTIFY that the foregoing correspondence has been forwarded via facsimile number 571-273-8300 to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 this 11th day of October, 2005.